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EXAMINER	
WALTER, CRAIG E	
ART UNIT	PAPER NUMBER
2188	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,118	KIMURA ET AL.	
	Examiner	Art Unit	
	CRAIG E. WALTER	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-13,15-18,23-27,29,30,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-13,15-18,23-27,29,30,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-4, 9-13, 15-18, 23-27, 29, 30, 32 and 33 are pending in the Application.

Claims 1, 13, 15, 27, 29, 30, 32 and 33 have been amended.

Claims 5-8, 14, 19-22, 28 and 31 have been cancelled.

Claims 1-4, 9-13, 15-18, 23-27, 29, 30, 32 and 33 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 11 April 2008 in response to the office action mailed on 11 December 2007 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 32 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Avraham et al. (US PG Publication 2004/0103238 A1), hereinafter Avraham.

As for claim 32, Avraham teaches a method of efficiently using a mirrored cache, the method comprising:

determining whether a master area of a first memory module is insufficient for a data input request; and storing data associated with said data input request, in a mirror area of a second memory module when it is determined that said master area of said first memory module is insufficient for the data input request (paragraph 0054, all lines – Avraham teaches a second memory module as being written with all or part of a first memory module's data once it is determined that the first memory module is full - paragraph 0054, all lines). Simply stated, Avraham teaches a second memory module as being written with all of part of a first memory module's data once it is determined that the first memory module is full. Note, the data being transmitted from the first memory module to the second was "initially" directed to the master area (i.e. stored there prior to be sent to the second memory).

More specifically (referring again to paragraph 0054, all lines), the determining step is met once the system checks to see if the cache is full. That is, every time a new write request is received, the cache is checked to see if it is full (see Fig. 3). The storing step is met by Avraham's process step of transferring data from the volatile memory to the nonvolatile memory. That is, data that is stored in the volatile memory was originally "from the data input request" for it to be stored in the volatile memory, therefore the data stored in the nonvolatile memory (after the transfer from volatile to nonvolatile memory is complete) comprises data once directed to the master area of the first memory, from

the data input request from which a determination was made to see if the master area of the volatile memory was “sufficient”.

As for claim 33, Avraham teaches a storage control method comprising:

transferring data to two cache modules using two transferred-to addresses (paragraph 0054, all lines – data is transferred to a volatile memory, and subsequently to a non-volatile memory. The system must inherently use addressing information in order to access the memory locations, hence Avraham's method includes "using two transferred-to addresses") and;

storing data, associated with a data input request, in a mirror area of one cache module when a master area of the other cache module is insufficient for receiving the data associated with the data input request (paragraph 0054, all lines – Avraham teaches a second memory module as being written with all or part of a first memory module’s data once it is determined that the first memory module is full - paragraph 0054, all lines).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 13, 15, 27, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber (US Patent 5,937,174) in view of Hauck et al. (US PG Publication 2003/0158999 A1), hereinafter Hauck, and in further view of Avraham (US PG Publication 2004/0103238 A1).

As for claims 13, 27, and 30, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, combination of elements 204 and 206);

Weber further teaches:

a bridge module connected through an interface bus to said disk interface modules, without connecting through any other bridge modules, said host interface module and said management modules for making connections among said disk interface module (Fig. 2, element 208 – the connections between the memory and the host are busses 252 and 250), the bridge module producing address information for two transferred-to addresses for the data written to the at least two second modules of the plurality of second modules – note data, commands and addressing information must be sent through the bus bridge (208) to reach the disks. In other words, the addressing information is "produced" by the bus bridge before it reaches the memory).

said host interface module and said management modules for data transfer among said modules, said host interface module writing data to be written, which is received from said host, through said bridge module into cache memories of two of said plurality of management modules (referring again to Fig. 2, the host can communicate with the storage module (element 104, which contains multiple modules or drives) via the host interface, the bridge and the disk interfaces (combination of elements 204 and 206, 208 and 138.1 respectively)) - col. 7, line 47 through col. 8, lines 39. It is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as will be discussed *infra*.

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ... 118). Referring to Fig. 2, each control unit (i.e. controller) contains a Read Write Cache Area, and a Cache Copy Area – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Weber additionally fails to teach the management modules as containing cache with the ability to mirror data, however Hauck teaches each of said management

modules including management means (each controller is used to manage read/write functions to the cache) for managing information on the management module which is in mirror relation to this management module (referring to Fig. 2, Host Write #1 data (230) is written to controller 2 (i.e. mirrored), and likewise Host Write #2 data (270) is mirrored to controller 1 – paragraph 0039-0040 all lines). Hauck additionally teaches managing the association between a master area address in said cache memory in this management module and a mirror area address in said cache memory of the management module being in the mirror relation to this management module (referring to Fig. 4, a master area for each cache is maintained (Read/Write/Copy Cache)). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

Hauck additionally teaches in a case in which a capacity of a master area of said cache memory of the one second module is full when data read out from said disk unit through said disk interface module and said bridge module is temporarily preserved in the cache memory of the one second management module, the one second management module preserves the readout data in a mirror area of said cache memory of the other second management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data

from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

Lastly, neither Hauck nor Weber teach a master area of said one second module is written to until the master area of said one second module is full, at which time a mirror area of said other second module is written to.

Avraham however teaches an appliance including a FLASH memory in which a second memory module is written with all or part of a first memory module's data once it is determined that the first memory module is full (paragraph 0054, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory

in to his own scalable memory. By doing so, Weber would have a more robust memory system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

As for claims 1, 15, and 29, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, the combination of elements 204 and 206);

Weber further teaches:

a bridge module connected through an interface bus to said disk interface module without connecting through any other bridge modules, said host interface module and said management modules for making connections among said disk interface module, said host interface module and said management modules for data transfer among said modules (Fig. 2, element 208 – the connections between the memory and the host are busses 252 and 250),

said bridge module including:

address production means for analyzing said addressing information, which is received together with said data to be written from said host interface module, to produce two transferred-to addresses for designation of said two management modules having said cache memories in which said data is to be

actually written and to produce written-in addresses in said cache memories (col. 8, lines 20-39) – the bridge unit works in conjunction with the host interface and the memory controller. The bridge unit receives data and address from the host interface and memory controller in order to communicate with (i.e. perform memory access functions on) the memory subsystem. The interface and memory controller help to permit the bridge to get the correct data to the correct locations on the disks within the subsystem. Note data, commands and addressing information must be sent through the bus bridge (208) to reach the disks. In other words, the addressing information is "produced" by the module before it reaches the memory; and

data transfer control means for controlling data transfer from said bridge module to said management modules so that, after said data is transferred to the two management modules corresponding to said two transferred-to addresses, said data is written at said written-in address in said cache memory of each of the two management modules (Fig. 2, the host (108) can write and read data to and from the storage system via the host interface (the combination of 204 and 206) to the bridge (208), through the device interface (138.1) – col. 7, line 47 through col. 8, lines 39). Again, it is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as per the discussion *supra* (per claims 13 and 27). When the host writes to the storage system, the

data is mirrored in Hauck's system such that at least two addresses (one for each controller's cache) are written-in to.

Weber additionally teaches one of the two management modules as including management means for managing information on the management module which is in mirror relation to the other management module and for managing the association between a master area address in said cache memory of the one second management module and a mirror area address in said cache memory of the other second management module being in the mirror relation to this management module - referring to Fig. 2, host write 1 data (230) is written to controller 2 (i.e. mirrored), and likewise host write data 2 (270) is mirrored to controller 1 – paragraph 0039-0040 all lines. Additionally, Weber teaches (referring to Fig. 4) a master area for each cache is maintained (Read/Write/Copy Cache). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 … 118,

120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, … 118). Referring to Fig. 2, each control unit (i.e. controller) contains a cache area (270), and a cache copy area (280) – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Neither Hauck nor Weber teach a master area of said one second module is written to until the master area of said one second module is full, at which time a mirror area of said other second module is written to.

Avraham however teaches an appliance including a FLASH memory in which a second memory module is written with all or part of a first memory module's data once it is determined that the first memory module is full (paragraph 0054, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory

in to his own scalable memory. By doing so, Weber would have a more robust memory system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

5. Claims 2-4, 9-12, 16-18 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Weber (US Patent 5,937,174), Hauck (US PG Publication 2003/0158999 A1), and Avraham (US PG Publication 2004/0103238 A1) as applied to claims 1 and 15 above respectively, and in further view of Hashimoto et al. (US PG Publication 2002/0016898 A1), hereinafter Hashimoto.

As for claims 2-3 and 16-17, though the combined teaches of Weber, Hauck and Avraham teach all the limitations of claim 1 and 15 above, they fails to teach the limitations of claims 2 and 3. Hashimoto further teaches designating, in said addressing information, a page address in said cache memory of each of said management modules and an offset address in a page designated by said page address, as said written-in address for said data in said cache memory, and specific information for specifying said two management modules having said cache memories in which said data is to be actually written, as said two transferred-to addresses for said data (Hashimoto discusses address conversion circuitry for both the first and second addresses. The address conversion circuitry uses the generated address and an offset (inherent for the conversion to take place) to generate appropriate addresses, in order to access the memories, paragraph 0019-0020, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his

own memory structure for high data bandwidth RAID applications. By doing so, Weber would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 4 and 18, Weber teaches interface bus is a PCI (Peripheral Component Interconnect) bus, and numbers for specifying said PCI bus for said two management modules are designated as said specific information (col. 8, lines 20-39).

It is worthy to note that since Weber only teaches one bus line, the addresses generated by Hashimoto could only refer to the one address bus that is used to transfer the data specified by the generated addresses.

As for claims 9-12 and 23-26, Hauck teaches a case in which a capacity of a master area of said cache memory is full when data read out from said disk unit through said disk interface module and said bridge module is temporarily preserved in the cache memory, each of said management modules preserves the readout data in a mirror area of said cache memory of the management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

Response to Arguments

6. Applicant's arguments have been fully considered however they are not persuasive.

Under the heading, "REJECTIONS OF CLAIMS 32-33 UNDER 35 U.S.C. § 102", Applicant asserts contrasts Avraham's teachings to the instant claims, and suggests that Avraham fails to teach "when the master area of a first memory module is determined to be insufficient for data associated with a data input request, the data is instead stored in a mirror area of a second memory module".

This argument however is not persuasive. The claim sets forth a process comprising two steps. A determining step to determine if a master area of a first memory module is "sufficient" for an input request; and a storing step, which stores data

directed to the master from the input request, to a mirrored area of a second memory module. For example (referring again to paragraph 0054, all lines), the determining step is met once the system checks to see if the cache is full. That is, every time a new write request is received, the cache is checked to see if it is full (see Fig. 3). Therefore, the data stored in the master area (associated with the input request) is transferred to the mirror area only after it is determined that the master area is no longer sufficient in size. As such, Avraham anticipates claims 32 and 33 as per the arguments and rejections discussed *supra*.

Under the heading, "REJECTIONS OF CLAIMS 1-4,9-13,15-18,23-27 AND 29-30 UNDER 35 U.S.C. § 103", Applicant contends that these claims are allowable for similar reasons as set forth in claims 32 and 33 (Avraham allegedly not teaching those elements in common with claims 32 and 33).

This argument however is not persuasive as Examiner maintains as per the rejection and Examiner's response above, that Avraham does in fact teach storing data associated with the data input request in a mirror area of a second memory module when it is determined that said master area of said first memory module is insufficient for the data input request.

Applicant finally asserts that all dependant claims are allowable for at least further limiting the base claims which are alleged to overcome the cited art. This argument however is not persuasive, as Examiner maintains that each base claim is rendered obvious by the cited art as per the rejections and arguments discussed supra.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CRAIG E. WALTER whose telephone number is (571)272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188
06/30/08

/Craig E Walter/
Patent Examiner, Art Unit 2188

CEW